SINGLE AND DUAL GATE GaAs FET INTEGRATED AMPLIFIERS IN C BAND

S. Arnold
Plessey Avionics and Communications Research Laboratory,
Roke Manor, Romsey, Hampshire, England.

Abstract

This paper outlines some aspects of the device characterisation, circuit design and realisation of hybrid integrated amplifiers in C Band. The performance of designs at 5 GHz employing single and dual-gate GaAs FETs are presented.

Introduction

Hybrid integrated amplifiers using single and dual gate GaAs field effect transistors have been designed for use in experimental C-band landing and navigational aids being investigated at the Royal Aircraft Establishment, Farnborough, U.K. These amplifiers have been designed to satisfy simultaneously a number of performance criteria; in particular, two designs to meet a 20 dB gain requirement at 5 to 5.25 GHz with min VSWR, group delay variation and noise figure are presented. Designs were realised in alumina microstrip incorporating unencapsulated active devices, film capacitors on semiconductor substrates and thin film resistors. No trimming facility existed in the amplifiers and accuracy was essential in each phase of the design. The general design procedure crystallises well into three distinct, though interdependent phases; namely device characterisation, circuit design and realisation.

Characterisation

With gain at a premium, it was necessary to use unencapsulated FETs in order to reduce parasitics, both during assessment and in the final circuit. A standard format for interfacing the device with stripline was formulated subject to the requirement that a final amplifier would faithfully repeat the encapsulation constraints present in characterisation. The fully corrected two-port measurements which form the raw material of the design stage were, therefore, of a device with a given set of mounting parasitics. The basic mounting structure of a 2μm single gate device is shown in figure 1. Through power coupling of orthogonal input and output lines with no device is less than -30 dB up to X Band. The earthing strip is connected to the ground plane at the test ceramic edge and a 1.5 mm wide strip maintains coupling at the -30 dB level in C Band. The FETs are on semi-insulating substrates and were bonded with resin directly to the ceramic. The test ceramic edges were ground to slide into the jig beneath the connector tabs, which were then held under pressure.

The same basic format was used for dual gate FET measurement. With the first gate grounded, preliminary 4μm dual gate FET characterisation has suggested a cascode operation subject to the conditions that a suitable reactance is presented to the second gate terminal and that this is biased at approximately half the drain potential. The bonding wire connecting the second gate to ground formed a lumped reactance, the value of which was optimized for gain at 5 GHz. This gain exceeded that in a corresponding 4μm gate common source - common gate pair.

Devices were characterised by S-parameter measurements. These were corrected for the small discontinuities existing between the network analyser and device terminals by comparison with characterised microstrip standards referred to the device terminals. The microstrip to co-axial interface could be formed with high reproducibility and the standards, also ground to fit, were slid sucessively into the jig. Microstrip open circuits most closely approximate their theoretical counterpart and replaced the normal short circuit and offset short circuit standards. A 50 ohm through line of electrical length equal to the two arms of the test ceramic formed the third mircostrip standard and the network analyser coupler errors could still be characterised using a co-axial sliding matched load.

In order to assess the degradation in performance of the mounting format chosen compared with an intrinsic device, three port S parameter characterisation was performed. A similar approach was made to the correction of these measurements and MAGs obtained from two and three port characterisation were compared for a common source 2μm single gate device; the results were similar, figure 2.

Circuit Design

The active device dictates to some extent amplifier topology. Beyond the normal requirement that the circuit must be consistent with introducing bias, designs had to conform with the basic device format. Techniques of numerical circuit optimisation currently available normally require initialisation of element values within a specified topology. These estimates and also the general interstage matching circuit topology were established from inspection of device parameters supplemented by analysis routines.

Target gains were estimated from the device MAG when unconditionally stable, or extrapolated values from such regions if only conditionally stable. The optimum theoretical match over the band was estimated and this was used to establish realistic weighting of gain, gain ripple and match conditions, these being the criteria of optimisation. Source and load impedances for minimum noise figure were almost identical with conjugate match conditions. Out of band performance was included in the minimisation only when instability was encountered or imminent. Though the circuit design phase was predominantly theoretical, halts were constantly made to take account of compatability with the physical constraints imposed in realisation of the design. In this manner the theoretical design was guided toward realisability often striking a compromise with performance; in particular, the high impedances of the FET usually provided difficulty in obtaining broad band designs.

Realisation

Bias isolation and r.f. decoupling was most readily accomplished with Al/SiO_2/GaAs chip capacitors and 20 pf

capacitors on 0.4 mm square dice with 12 V breakdown offered dimensional compatibility with the designs. The equivalent capacitor circuit and microstrip loss was incorporated into the optimisation and compensation for discontinuity in the transmission lines was introduced in the final layout.

Figure 3 shows the theoretical performance of a pair of single gate, three stage 10 dB amplifier modules when connected together. Modules are identical, each comprises one common source and two common gate stages, and are matched to 50 ohms. This basic module contains the minimum number of stages to provide adequate gain and acceptable VSWRs, thereby simplifying the design and amplifier check out. Final substrates were probe tested and any defective devices identified and replaced; in general device uniformity was good. The final laboratory model amplifiers comprising two of the 10 dB gain blocks shown in figure 4 exhibited close agreement with theory, figure 3. Amplifier noise figures were 0.5 dB above the theoretical minimum for the devices initially used and with subsequent selection of first stages noise figures should be at the 7 dB level. A theoretical, though realisable, amplifier design similar to the single gate design but with dual gate devices replacing the common gate stages has been completed. The superior performance achieved in this amplifier, figure 5, spells a bright future for the microwave dual gate FET.

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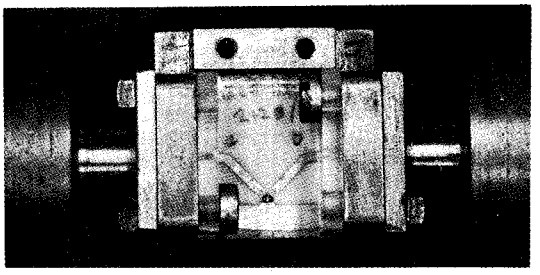

Fig. 1 FET Microstrip Mounting Structure

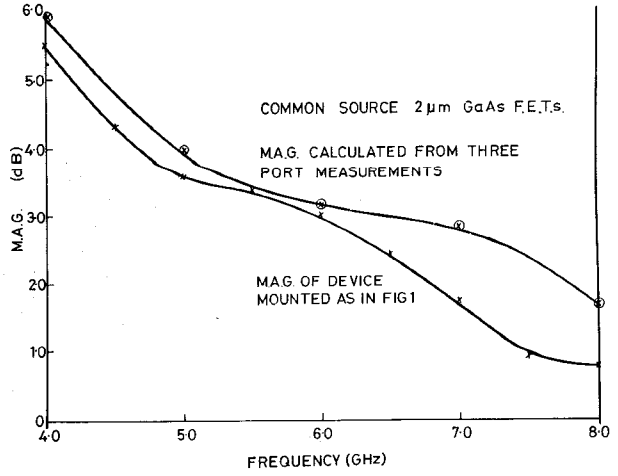

Fig. 2 2 and 3 Port S-Parameter Characterisation

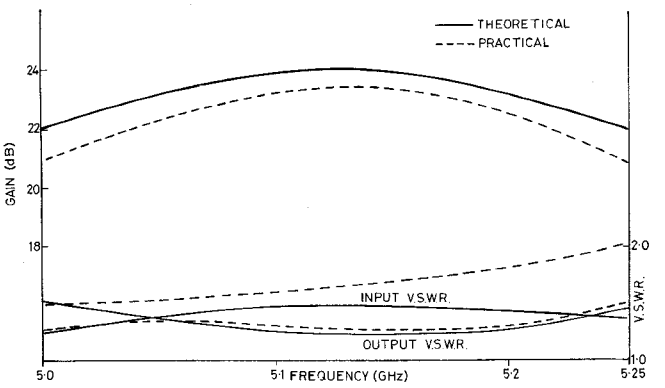

Fig. 3 Two Module 20 dB Single Gate Amplifier

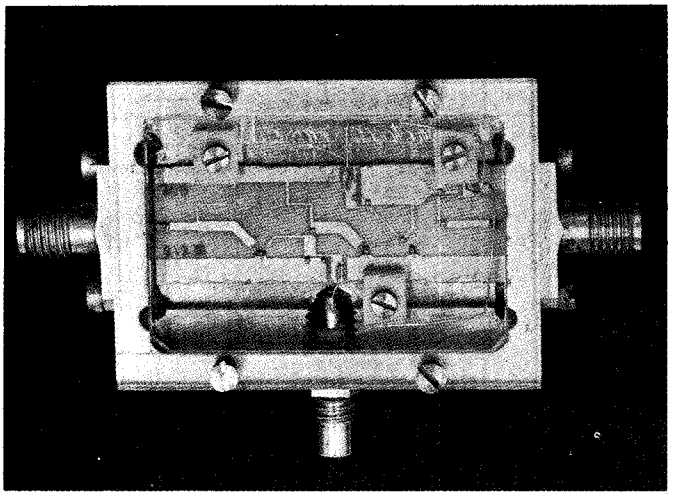

Fig. 4 Single Module 2μm Single Gate FET 5.0 - 5.25 GHz Amplifier

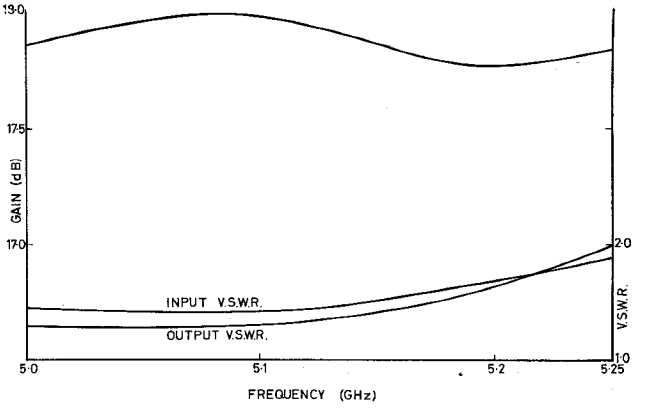

Fig. 5 Single Module Single and Dual Gate Amplifier